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1 **A novel CMOS compatible multi-level flash EEPROM for embedded applications**
Concannon, A.; McCarthy, D.; Mathewson, A.; Guillaumot, B.; Papadas, C.; Kelaidis, C.;
Device Research Conference Digest, 1998. 56th Annual , 22-24 June 1998
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[Abstract]   [PDF Full-Text (364 KB)]   **IEEE CNF**

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Myung Kwan Cho; Kim, D.M.;
Electron Device Letters, IEEE , Volume: 21 , Issue: 8 , Aug. 2000
Pages:399 - 401

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3 **Fast and accurate programming method for multi-level NAND EEPROMs**
Hemink, G.J.; Tanaka, T.; Endoh, T.; Aritome, S.; Shirota, R.;
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4 **Functionally separated, multiple-valued content-addressable memory and its applications**
Hanyu, T.; Aragaki, S.; Higuchi, T.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 142 , Issue: 3 , June 1995
Pages:165 - 172

[Abstract]   [PDF Full-Text (516 KB)]   **IEE JNL**

5 **Variable stress-induced leakage current and analysis of anomalous charge loss for flash memory application**
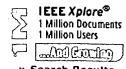*Yamada, R.; King, T.J.;*

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1 **Multiple-valued floating-gate-MOS pass logic and its application to logic-in-memory VLSI**
Hanyu, T.; Teranihi, K.; Kameyama, M.;
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3 **Multiple-valued logic-in-memory VLSI based on a floating-gate-MOS pass-transistor network**
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